REMARKS/ARGUMENTS

In the claims

Claims 1-9 remain in this application.

35 U.S.C. 102(e)

Claims 1-9 are rejected under 35 U.S.C. 102 (e) as being anticipated by Horvath et al (US Patent 6,754,745).

Claim 1 recites a method for synchronizing all clock sources of semiconductor devices comprising (a) generating multiple clock sources in a plurality of semiconductor devices (b) designating one semiconductor device having a clock source with the lowest rate clock signal as a master device and other devices as slave devices when the multiple clock sources are stable (c) designating the lowest rate clock signal of the master device as a reference clock source (d) performing, according to the reference clock source, a phase-aligned check on other clock sources in the master device, such that other clock sources of the master device are synchronized with the reference clock source to generate a zeroing signal (e) respectively performing, according to the zeroing signal, a phase-aligned check on a local lowest rate clock source in each slave device, such that all local lowest rate clock sources of the slave devices are synchronized with the lowest rate clock signal of the master device to respectively generate an aligning signal and (f) respectively performing, according to the aligning signal, a phase-aligned check on other clock sources in each slave device, such that other clock sources of each slave device are separately synchronized with the local lowest rate clock signal of the respective slave devices, thereby completing clock synchronization for the plurality of semiconductor devices.

Horvath does not teach or suggest "other clock sources of the master device are synchronized with the reference clock source to generate a zeroing signal (e) respectively performing,

according to the zeroing signal, a phase-aligned check on a local lowest rate clock source in each slave device".

Horvath discloses that voice server 601 provides the 8KHz reference clock to other cards 602, 603 and 604, but fails to teach or disclose that the zeroing signal is generated when other clock sources of the master device are synchronized with the reference clock source and according to the zeroing signal slave device performs phase-aligned check on a local lowest rate clock source. As shown in Fig. 6 of Horvath, voice server 601 apparently does not generate any signal when other clock sources of the voice server 601 are synchronized with the reference clock. PLL 620 is a device for providing transmit the clock and MUX 613 is a device for selecting two inputs. Therefore, Horvath does not teach or disclose that other clock sources of the master device are synchronized with the reference clock source to generate a zeroing signal. In addition, since the zero signal is not generated, Horvath does not teach or disclose that a phase-aligned check is respectively performed on a local lowest rate clock source in each slave device according to the zeroing signal as claimed by claim!

For the reasons described above, Applicant believes that claim 1 is allowable over the cited reference.

In addition, Horvath does not teach or suggest "all local lowest rate clock sources of the slave devices are synchronized with the lowest rate clock signal of the master device to respectively generate an aligning signal and (f) respectively performing, according to the aligning signal, a phase-aligned check on other clock sources in each slave device, such that other clock sources of each slave device are separately synchronized with the local lowest rate clock signal of the respective slave devices".

Horvath discloses that other cards 602, 603 and 604 receive the 8KHz reference clock from voice server 601 and provides the transmit clock on all the ports to be synchronized with the 8KHz reference clock, but fails to teach or disclose that an aligning signal is generated when all local lowest rate clock sources of the slave devices are synchronized with the lowest rate clock signal of the master device and according to the aligning signal the slave device perform a phase-aligned check on other clock sources. As shown in Fig. 6 of Horvath, voice server 603 does not generate any signal when other clock sources of the voice server 603 are synchronized with the reference clock from backplane 605, PLL is an analog device for providing transmit clock and OSC 695 is a device for providing clock. Therefore, Horvath does not teach or disclose that all local lowest rate clock sources of the slave devices are synchronized with the lowest rate clock signal of the master device to respectively generate an aligning signal. In addition, since the aligning signal is not generated, Horvath does not teach or disclose that a phase-aligned check is respectively performing on other clock sources in each slave device according to the aligning signal.

For the reasons described above, Applicant believes that claim 1 is allowable over the cited reference.

Thus, Applicant believes that claim 1 is allowable over the cited references. Insofar as claim 1 is allowable, claims 2-6, all depend from claim 1 and its related claims, including every claimed element thereof, are also allowable on their own merits in claiming additional elements not included in claim 1.

Claim 4 recites step (d) further comprising (d1) triggering a phase checker in the master device to sample the clock sources inside the master device for phase alignment comparison by means of rising or falling edges of an external input clock source, (d2) outputting the zeroing

signal to concurrently signal each slave device when all phases are aligned and (d3) otherwise, outputting a reset signal reset to re-generate multiple clock sources for re-alignment operation.

Horvath does not teach or suggest "(d2) outputting the zeroing signal to concurrently signal each slave device when all phases are aligned, and (d3) otherwise, outputting a reset signal reset to re-generate multiple clock sources for re-alignment operation".

Horvath only discloses that voice server 601 provides the transmit clock to be synchronized with the 8KHz reference clock, but fails to teach or disclose outputting the zeroing signal to concurrently signal each slave device when all phases are aligned or outputting a reset signal reset to re-generate multiple clock sources for re-alignment operation.

For the reasons described above, Applicant believes that claim 4 is allowable over the cited reference.

Claim 5 recites step (e) further comprising (e1) respectively checking the lowest rate clock source of the master device through an external phase checker in each slave device to determine if the zeroing signal has been sent, (e2) respectively performing a phase-aligned check on each slave device through a respective external phase checker when the zeroing signal is received and all clock sources in each slave device are stable, (e3) respectively sending the aligning signal to indicate a phase alignment and clock synchronization for the lowest rate clock signal of the master device and the local lowest rate clock signal of the respective slave device when all phases are aligned and (e4) otherwise, sending a reset signal to re-generate the local lowest rate clock signal of the respective slave device and then repeat step (e1).

Horvath does not teach or suggest "(e3) respectively sending the aligning signal to indicate a phase alignment and clock synchronization for the lowest rate clock signal of the master device and the local lowest rate clock signal of the respective slave device when all phases are aligned, and (e4) otherwise, sending a reset signal to re-generate the local lowest rate clock signal of the respective slave device and then repeat step (e1)".

Horvath only discloses that other cards 602, 603 and 604 receive the 8KHz reference clock from voice server 601 and provides the transmit clock on all the ports to be synchronized with the 8KHz reference clock, but fails to teach or disclose how to synchronize between master device and the salve device by sending the aligning signal or the reset signal.

For the reasons described above, Applicant believes that claim 5 is allowable over the cited reference.

Claim 6 recites step (f) further comprising (f1) respective internal phase checkers in each slave device determining if a respective external phase checker has sent the aligning signal, (f2) respective internal phase checkers performing the phase-aligned check in a respective slave device when the aligning signal is received and all clock sources in the respective slave device are stable, (f3) sending the aligning signal to indicate a phase alignment for the clock sources in the respective slave device and a clock synchronization for the semiconductor devices when all phases are aligned and (f4) otherwise, sending a reset signal reset to respectively re-generate the multiple clock sources, except the local lowest rate clock source, of the respective slave device and then repeat step (f1).

Where does Horvath teach or suggest "(f3) sending the aligning signal to indicate a phase alignment for the clock sources in the respective slave device and a clock synchronization for the

semiconductor devices when all phases are aligned and (f4) otherwise, sending a reset signal re-set to respectively re-generate the multiple clock sources, except the local lowest rate clock source, of the respective slave device and then repeat step (f1)"?

Horvath discloses that other cards 602, 603 and 604 receive the 8KHz reference clock from voice server 601 and provides the transmit clock on all the ports to be synchronized with the 8KHz reference clock, but fails to teach or disclose how to synchronize that sending the aligning signal indicates a phase alignment for the clock sources in the respective slave device and a clock synchronization for the semiconductor devices when all phases are aligned.

For the reasons described above, Applicant believes that claim 6 is allowable over the cited reference.

Claim 7 recites a system for synchronizing all clock sources of semiconductor devices comprising a first semiconductor device having a phase checker and a multi-clock generator including generation of the lowest rate clock source, wherein the phase checker performs phase alignment according to the lowest rate clock source, such that multiple clock sources generated by the multi-clock generator are synchronized and thus a zeroing signal is output, a plurality of second semiconductor devices, each having an external phase checker, an internal phase checker and a multi-clock generator including generation of a clock-aligned source, wherein the external phase checker performs phase alignment according to the zeroing signal, such that the lowest rate clock source and the clock-aligned source have phase synchronization to thus output an aligning signal to the internal phase checker for phase alignment, thereby synchronizing multiple clock sources generated by each second semiconductor, and thus completing clock synchronization of all semiconductor devices.

Where does Horvath teach or suggest "a plurality of second semiconductor devices, each having an external phase checker, an internal phase checker and a multi-clock generator including generation of a clock-aligned source, wherein the external phase checker performs phase alignment according to the zeroing signal, such that the lowest rate clock source and the clock-aligned source have phase synchronization to thus output an aligning signal to the internal phase checker for phase alignment, thereby synchronizing multiple clock sources generated by each second semiconductor, and thus completing clock synchronization of all semiconductor devices"?

Horvath discloses that other cards 602, 603 and 604 receive the 8KHz reference clock from voice server 601 and provides the transmit clock on all the ports to be synchronized with the 8KHz reference clock, but fails to teach or disclose that each semiconductor device has an external phase checker and an internal phase checker. As shown in Fig. 6, voice server 601 and other cards 602, 603 and 604 use a PLL to provide a transmit clock but does not generate any zeroing signal when synchronization. Horvath also fails to teach or disclose that the external phase checker performs phase alignment according to the zeroing signal. The zeroing signal can be an output when the multiple clock source is synchronized. In addition, Horvath fails to teach or disclose that outputting an aligning signal to the internal phase checker for phase alignment. The alignment signal is output when the lowest rate clock source and the clock-aligned source have phase synchronization.

For the reasons described above, Applicant believes that claim 7 is allowable over the cited reference.

Thus, Applicant believes that claim 7 is allowable over the cited references. Insofar as claim 7 is allowable, claims 8-9, all depend from claim 7 and its related claims, including every

claimed element thereof, are also allowable on their own merits in claiming additional elements not included in claim 7.

Conclusion

For the reasons as described above, Applicant believes that claims 1, 4, 5, 6 and 7 are allowable over the cited references. Insofar as claim 1 is allowable, claims 2-6, all depend from claim 1 and its related claims, including every claimed element thereof, are also allowable on their own merits in claiming additional elements not included in claim 1. Moreover, for the reasons as described above, Applicant believes that claim 7 is allowable. Insofar as claims 8-9 depend from claim 7 and its related claims, they are also allowable.

Should Examiner feel that further discussion of the application and the Amendment is conducive to prosecution and allowance thereof, please do not hesitate to contact the undersigned at the address and telephone listed below.

The Commissioner is authorized to charge any additional fees which may be required or credit overpayment to deposit account no. 12-0415. In particular, if this response is not timely filed, then the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136 (a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 12-0415.